

Patent

Customer No.: 31561
Docket No. 12681-US-PA
Application No.: 10/708,171

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Applicant : Su et al.
Application No. : 10/708,171
Filed : 2004/2/12
For : ELECTRO-STATIC DISCHARGE PROTECTION CIRCUIT
FOR DUAL-POLARITY INPUT/OUTPUT PAD
Art Unit : 2815
Examiner : WARREN MATTHEW E

TRANSMITTAL LETTER

002-1-703-872-9306

(Via fax: 1+ 9 pages)

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DEC 28 2004

Assistant Commissioner for Patents
Arlington, Virginia 22202

Dear Sir,

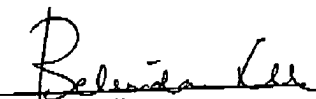
In response to the Office Action dated October 4, 2004 (Paper No.: 20041001), please find the *Response to Office Action*, in 9 pages.

I believe that no fee is incurred. However, the Commissioner is authorized to charge any fees required in connection with the filing of this paper to account No. 50-2620 (Order No.: 12681-US-PA)

Thank you for your assistance in the subject matter. If you have any questions, please feel free to contact me.

Respectfully Submitted,
JIANQ CHYUN Intellectual Property OfficeDate: Dec. 28, 2004

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Customer No.: 31561
Application No: 10/708,171
Docket NO.:12681-US-PA

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application)
Application	10/708,171
Filed:	February 12, 2004
For:	ELECTRO-STATIC DISCHARGE PROTECTION CIRCUIT FOR
	DUAL-POLARITY INPUT/OUTPUT PAD
Applicant:	Shin Su
Examiner:	Warren, Matthew E.
Art Unit	2815

No fee is believed to be due. However, the Commissioner is authorized to charge any fees required in connection with the filing of this paper to account. No.50-2620 (order No. 12681-US-PA

RESPONSE TO OFFICE ACTION

U.S. Patent and Trademark Office
Commissioner for Patents
220 20th Street South
Customer Window, Mail Stop Amendment
Crystal Plaza Two, Lobby, Room 1B03
Arlington, Virginia 22202

Dear Sir:

The Office Action mailed on October 04, 2004 has been carefully considered. In response thereto, please enter the following amendments and consider the following remarks.

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Claim Amendment

Please amend the claims according to the following listing of claims and substitute it for all prior versions and listings of claims in the application.

1. (currently amended) An electro-static discharge (ESD) protection circuit for a dual polarity input/output (I/O) pad, comprising:
 - a substrate of a first conductive type;
 - a deep well region of a second conductive type, disposed in the substrate of the first conductive type;
 - a well region of the first conductive type, disposed in the deep well region of the second conductive type;
 - a first transistor, disposed over the well region of the first conductive type, wherein the first transistor comprises a first gate, a first source and a first drain;
 - a second transistor, disposed over the substrate of the first conductive type, wherein the second transistor comprises a second gate, a second source and a second drain, wherein the second source is connected with the first drain, and wherein the second source and the first drain is disposed in a portion of the first conductive type well region, a portion of the second conductive type deep well region and a portion of the first conductive type substrate;

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a first doped region, disposed in the well region of first conductive type and laterally adjacent to the first source, wherein the first doped region, the first source and the first gate are electrically connected to an input pad; and

a second doped region, disposed in the substrate of the first conductive type and laterally adjacent to the second drain, wherein the second doped region, the second drain and the second gate are electrically connected to an output pad.

2. (currently amended) The electro-static discharge (ESD) protection circuit of claim 1, wherein the substrate of first conductive type comprises a p-type substrate.

3. (currently amended) The electro-static discharge (ESD) protection circuit of claim 1, wherein the deep well region of second conductive type comprises a n-type deep well region.

4. (currently amended) The electro-static discharge (ESD) protection circuit of claim 1, wherein the well region of first conductive type comprises a p-type well region.

5.(original) The electro-static discharge (ESD) protection circuit of claim 1, wherein the first transistor and the second transistor comprise a NMOS transistor.

6. (original)The electro-static discharge (ESD) protection circuit of claim 1, wherein the first doped region and the second doped region comprise a p-type doped region.

7. (currently amended) The electro-static discharge (ESD) protection circuit of claim 1, wherein when the input pad receives a positive electro-static current, a first parasitic bipolar junction transistor is formed by the first conductive type well region, the second type deep well region and the first conductive type substrate, and a second parasitic bipolar junction transistor

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is formed by the second conductive type deep well region, the first conductive type substrate and the second drain, and a positive feedback loop is formed by the first parasitic bipolar junction transistor and the second parasitic bipolar junction transistor.

8. (currently amended) The electro-static discharge (ESD) protection circuit of claim 1, wherein when the input pad receives a negative electro-static current, a first parasitic bipolar junction transistor is formed by the first conductive type substrate, the second conductive type deep well region and the first conductive type well region, and a second parasitic bipolar junction transistor is formed by the second conductive type deep well region, the first conductive type well region and the first source, and a positive feedback loop is formed by the first parasitic bipolar junction transistor and the second parasitic bipolar junction transistor.